INTEGRATED CIRCUITS

**RS 7400**

**QUADRUPLE TWO-INPUT NAND GATE**

**GENERAL DESCRIPTION**

Employing TTL (Transistor-Transistor-Logic) to achieve high speed at moderate power dissipation, these gates provide the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature.

**FEATURES**

- Guaranteed Noise Immunity 400 mV
- Typical Noise Immunity 1V
- Average Propagation Delay 13 ns
- Fan Out 10
- Average Power Dissipation 10 mW per gate

**ABSOLUTE MAXIMUM RATINGS**

- $V_{CC}$..............................................7.0V
- Input Voltage.....................................5.5V
- Storage Temperature Range..............-65°C to +150°C
- Fan-Out...........................................10
- Lead Temperature (Soldering, 10 sec)...............300°C
- Supply Voltage ($V_{CC}$)..........................4.75–5.25V
- Temperature ($T_A$)..............................0°C to 70°C

**RS 7402**

**QUAD TWO-INPUT NOR GATE**

**GENERAL DESCRIPTION**

The 7402 is a quad 2-input NOR gate utilizing TTL (Transistor-Transistor Logic) to achieve high speed at nominal power dissipation.

**FEATURES**

- Input Clamping Diodes
- Guaranteed Noise Immunity 400 mV
- Typical Noise Immunity 1V
- Fan-out 10
- Allowable Power Supply Variation 4.75V to 5.25V
- Average Propagation Delay 12 ns (with 50 pF)
- Average Power Dissipation 14 mW per gate

**ABSOLUTE MAXIMUM RATINGS**

- $V_{CC}$..............................................7V
- Input Voltage.....................................5.5V
- Operating Temperature Range....................0°C to 70°C
- Storage Temperature Range.....................-65°C to +150°C
- Lead Temperature (Soldering, 10 sec)...............300°C

**RS 7404**

**HEX INVERTER**

**GENERAL DESCRIPTION**

The 7404 is a hex inverter utilizing TTL to achieve high speed at nominal power dissipation. It is totally compatible with other Series 74 devices.

**FEATURES**

- Input clamping diodes
- Guaranteed Noise Immunity 400 mV
- Typical Noise Immunity 1V
- Fan-out 10
- Allowable Power Supply Variation 4.75V to 5.25V
- Average Propagation Delay 12 ns (with 50 pF)
- Average Power Dissipation 10 mW per gate

**ABSOLUTE MAXIMUM RATINGS**

- $V_{CC}$..............................................7V
- Input Voltage.....................................5.5V
- Operating Temperature Range....................0°C to 70°C
- Storage Temperature Range.....................-65°C to +150°C
- Lead Temperature (soldering, 10 sec)...............300°C

COMPLETE DATA AND SPECIFICATIONS SUPPLIED WITH EACH DEVICE
HEX INVERTER BUFFER/DRIVER

**GENERAL DESCRIPTION**
The TTL hex inverter buffer/driver is fully compatible for use with TTL and DTL logic circuits. Each inverter features high-voltage, open-collector outputs (30 volts minimum breakdown.)

**FEATURES**
- Input clamp diodes
- 15 ns typical propagation delay time
- High voltage open-collector outputs 30V
- High sink current capability 40 mA

**ABSOLUTE MAXIMUM RATINGS**
- Supply Voltage: 7.0V
- Input Voltage: 5.5V
- Output Voltage: 30V
- Storage Temperature Range: -65°C to +150°C
- Lead Temperature (Soldering, 10 Sec): +300°C
- Supply Voltage: +4.75 to 5.25V
- Temperature (T_A): 0°C to 70°C
- Output Sink Current: +0.4 mA

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QUAD TWO-INPUT AND GATE

**GENERAL DESCRIPTION**
7408 provides the non-inverting AND function in the popular quad 2-input pin configuration.

**ABSOLUTE MAXIMUM RATINGS**
- Supply Voltage: 7V
- Input Voltage: 5.5V
- Output Voltage: 5.5V
- Storage Temperature Range: -65°C to +150°C
- Lead Temperature (Soldering, 10 sec): +300°C
- Supply Voltage (V_CC): +4.75 to 5.25V
- Temperature (T_A): 0°C to 70°C

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TRIPLE THREE-INPUT NAND GATE

**GENERAL DESCRIPTION**
Employing TTL (Transistor-Transistor-Logic) to achieve high speed at moderate power dissipation, these gates provide the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature.

**FEATURES**
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 10
- Average Propagation Delay 13 ns
- Average Power Dissipation 10 mW per gate

**ABSOLUTE MAXIMUM RATINGS**
- Supply Voltage (V_CC): 7.0V
- Input Voltage: 5.5V
- Storage Temperature Range: -65°C to +150°C
- Fan-Out: 10
- Lead Temperature (Soldering, 10 sec): +300°C
- Supply Voltage (V CC): +4.75 to 5.25V
- Temperature (T_A): 0°C to 70°C
### RS 7413

**276-1815**

**DUAL SCHMITT-TRIGGER**

**GENERAL DESCRIPTION**

The 7413 is a dual Schmitt-trigger with input gating. It differs from a conventional dual 4-input gate in that instead of having a single threshold voltage, the 7413 has different thresholds for positive- and negative-going inputs. When the output is in the logical “0” state an input must be lowered to 0.8 volts typically before the output changes state. Conversely in order to return to the logical “0” state the input must rise to 1.7V typically. This hysteresis is extremely beneficial in applications where slow rise and fall time signals are prevalent.

**FEATURES**
- 400 mV hysteresis typ.—higher noise immunity
- Operation from very slow ramp voltages
- Temperature compensated design
- Typical propagation delay—17 ns
- Typical power dissipation 12 mW per function

**APPLICATIONS**
- Pulse shaper
- Threshold detector

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>7V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>5.5V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec)</td>
<td>300°C</td>
</tr>
</tbody>
</table>

### RS 7420

**276-1809**

**DUAL FOUR-INPUT NAND GATE**

**GENERAL DESCRIPTION**

Employing TTL (Transistor-Transistor-Logic) to achieve high speed at moderate power dissipation, these gates provide the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature.

**FEATURES**
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 10
- Average Propagation Delay 13 ns
- Average Power Dissipation 10 mW per gate

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Vcc</td>
<td>7.0V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>5.5V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Fan-Out</td>
<td>10</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec)</td>
<td>300°C</td>
</tr>
<tr>
<td>Supply Voltage (VCC)</td>
<td>4.75–5.25V</td>
</tr>
<tr>
<td>Temperature (T_A)</td>
<td>0°C to 70°C</td>
</tr>
</tbody>
</table>

### RS 7427

**276-1823**

**TRIPLE THREE-INPUT NOR GATE**

**GENERAL DESCRIPTION**

The NOR gate described here is designed to provide additional versatility to the line of 74 functions. The 7427 has neither expandable inputs nor Strobe.

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>7.0V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>5.5V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 seconds)</td>
<td>300°C</td>
</tr>
<tr>
<td>Supply Voltage (VCC)</td>
<td>4.75–5.25V</td>
</tr>
<tr>
<td>Temperature (T_A)</td>
<td>0°C to 70°C</td>
</tr>
</tbody>
</table>

COMPLETE DATA AND SPECIFICATIONS SUPPLIED WITH EACH DEVICE
QUAD LATCH

GENERAL DESCRIPTION
This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The 7475 features complementary Q and over outputs from a 4-bit latch, and are available in 16-pin packages.

ABSOLUTE MAXIMUM RATINGS
Supply voltage $V_{CC}$ ........................................ 4.75—5.25V
Logic input 1 voltage ........................................... 2.0V Min.
Logic input 0 voltage ........................................... 0.8V Max.
Logic output 1 voltage ......................................... 2.4V Min.
Logic output 0 voltage ......................................... 0.4V Max.

LOGIC DIAGRAM (Each Latch)

TRUTH TABLE (Each Latch)

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>G</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
</tr>
</tbody>
</table>

H = High Level, L = Low Level, X = Don’t Care
Q0 = The level of Q before the High-to-Low Transition of G

DUAL JK MASTER/SLAVE FLIP-FLOP

GENERAL DESCRIPTION
Incorporates separate presets, clears, and clocks. Clock pulse controls inputs to master section, and also regulates coupling between master and slave sections.

ABSOLUTE MAXIMUM RATINGS
Supply voltage $V_{CC}$ ........................................ 4.75—5.25V
Logic input 1 voltage ........................................... 2.0V Min.
Logic input 0 voltage ........................................... 0.8V Max.
Logic output 1 voltage ......................................... 2.4V Min.
Logic output 0 voltage ......................................... 0.4V Max.

TRUTH TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PR CLR CLK J K</td>
<td>Q Q</td>
</tr>
<tr>
<td>L H X X X</td>
<td>H L</td>
</tr>
<tr>
<td>H L X X X</td>
<td>L H</td>
</tr>
<tr>
<td>L L X X X</td>
<td>H* H*</td>
</tr>
<tr>
<td>H H &amp; L L L</td>
<td>Q0 Q0</td>
</tr>
<tr>
<td>H H &amp; L L H</td>
<td>H L</td>
</tr>
<tr>
<td>H H &amp; L H H</td>
<td>L H</td>
</tr>
<tr>
<td>H H &amp; H H H</td>
<td>TOGGLE</td>
</tr>
</tbody>
</table>

Notes:
* & = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
* Q0 = the level of Q before the indicated input conditions were established
* TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

COMPLETE DATA AND SPECIFICATIONS SUPPLIED WITH EACH DEVICE
DESCRIPTION

The 7473 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 7473 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-TO-LOW transition. For the 7473, the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS73 is a negative edge-triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-TO-LOW Clock transition for predictable operation.

The Reset (\( \bar{R}_D \)) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the \( \bar{Q} \) output HIGH.

ORDERING CODE

<table>
<thead>
<tr>
<th>PACKAGES</th>
<th>COMMERCIAL RANGES</th>
<th>MILITARY RANGES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( V_{CC} = 5\text{V} \pm 5% \text{; } T_A = 0^\circ\text{C} \text{ to } +70^\circ\text{C} )</td>
<td>( V_{CC} = 5\text{V} \pm 10% \text{; } T_A = -55^\circ\text{C} \text{ to } +125^\circ\text{C} )</td>
</tr>
<tr>
<td>Plastic Dip</td>
<td>N7473N – N74LS73N</td>
<td>S5473F – S54LS73F</td>
</tr>
<tr>
<td>Ceramic Dip</td>
<td>N7473F – N74LS73F</td>
<td>S5473F – S54LS73F</td>
</tr>
<tr>
<td>Flatpack</td>
<td>S5473W</td>
<td>S54LS73W</td>
</tr>
</tbody>
</table>

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

<table>
<thead>
<tr>
<th>PINS</th>
<th>DESCRIPTION</th>
<th>54/74</th>
<th>54/74LS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP</td>
<td>Clock Input</td>
<td>2ul</td>
<td>4LSul</td>
</tr>
<tr>
<td>( \bar{R}_D )</td>
<td>Reset Input</td>
<td>2ul</td>
<td>3LSul</td>
</tr>
<tr>
<td>J, K</td>
<td>Data Inputs</td>
<td>1ul</td>
<td>1LSul</td>
</tr>
<tr>
<td>Q, ( \bar{Q} )</td>
<td>Outputs</td>
<td>10ul</td>
<td>10LSul</td>
</tr>
</tbody>
</table>

NOTE

Where a 5474 unit load (ul) is understood to be 45\( \mu \text{A} \text{ I}_{UL} \) and \( -1.5\text{mA} \text{ I}_{IL} \) and a 5474LS unit load (LSul) is 20\( \mu \text{A} \text{ I}_{UL} \) and \( -0.6\text{mA} \text{ I}_{IL} \).

PIN CONFIGURATION

LOGIC SYMBOL

LOGIC SYMBOL (IEEE/IEC)

3-92
SDLS011

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**Description**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of -65°C to 125°C. The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C.

**Function Table**

<table>
<thead>
<tr>
<th>PRE</th>
<th>CLR</th>
<th>CLK</th>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>Q'</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>H'</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>Q'</td>
<td>Q</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>TOGGLE</td>
<td>Q'</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Q'</td>
<td>Q</td>
</tr>
</tbody>
</table>

† The output levels in this configuration are not guaranteed to meet the minimum levels for $V_{OH}$ if the lows at preset and clear are near $V_{IL}$ minimum. Furthermore, this configuration is nonstatic; that is, it will not persist when either preset or clear returns to its inactive (high) level.

**Logic Symbol**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.